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In the Specification:

Please replace the paragraph beginning on page 8, line 5 with the following:

Refer now to Figure 4, which is a cross-sectional view of wafer 100 after via 120 has been lined with two layers. Layer 125 consists of a thin dielectric layer, preferably 0.05 to 0.10 microns of SiO_2. This layer acts as an electrical insulator to prevent shorting between the metal layer of the filled via and components in the integrated circuit layer 112. The second layer 126 consists of a thin layer of SiN, typically 0.05 to 0.10 microns in thickness. The SiN layer serves two functions. First, it provides a diffusion barrier that helps to prevent the metal used to fill via 120 from diffusing into the integrated circuit layer if the primary diffusion barrier discussed below fails. Second, the silicon nitride provides an etch stop for the chemical etching processes used in the thinning of the silicon wafer. For example, the silicon can be thinned using a wet chemical process such as a substituted ammonium hydroxide or other alkaline chemical ~~etches~~ etch. It should also be noted that this etch stop will provide some resistance to acidic etch solutions. In this case, the silicon nitride acts as the etch stop. If a dry etch such as a Cl_2 based plasma chemistry is used to thin silicon, the SiO_2 layer can be used as an etch stop.